We claim:

1. An integrated semiconductor circuit, comprising:

a random signal generator having an output for supplying a random signal;

at least one controllable switching device having a control input connected to said output of said random signal generator;

a plurality of circuit units having respective clock inputs;

at least one terminal for supplying at least one clock signal, said clock inputs of said circuit units being connected to said at least one terminal via said at least one controllable switching device; and

said circuit units being controlled by the at least one clock signal and being configured to be operable in parallel and in series, at least one of said circuit units selectively operating in parallel and in series with at least another one of said circuit units based on the random signal.

2. The integrated semiconductor circuit according to claim 1, including:

at least one controllable clock signal generator having a control input connected to said output of said random signal generator, said at least one controllable clock signal generator being controlled such that an instant of a switching edge of the at least one clock signal varies based on the random signal; and

said at least one terminal for supplying the at least one clock signal being a clock signal output of said at least one controllable clock signal generator.

3. The integrated semiconductor circuit according to claim 1, wherein:

said at least one terminal for supplying the at least one clock signal includes at least a first terminal for supplying a first clock signal and a second terminal for supplying a second clock signal; and

a first number of said circuit units are operated with the first clock signal and a second number of said circuit units are operated with the second clock signal.

4. The integrated semiconductor circuit according to claim 3, wherein:

said at least one controllable switching device is a plurality of switching devices embodied as multiplexers; and

each of said multiplexers is supplied with the at least first and second clock signals and connects one of the at least first and second clock signals to a respective one of said circuit units based on the random signal.

5. The integrated semiconductor circuit according to claim 2, wherein said at least one controllable clock signal generator includes a voltage controlled oscillator.

6. The integrated semiconductor circuit according to claim 2, wherein said at least one controllable clock signal generator includes a phase locked loop with a frequency divider controlled by the random signal generator.

7. The integrated semiconductor circuit according to claim 1, wherein at least one of said circuit units is an auxiliary circuit unit.

8. A method for operating a clocked integrated semiconductor circuit, the method which comprises:

executing, in circuit units of an integrated semiconductor circuit, operations which each require a respective given number of clock signal periods; and

determining, based on a random signal, a further number of clock signal periods;

supplying the further number of clock signal periods to an auxiliary circuit unit having substantially a same current consumption as the circuit units; and

performing the supplying step at least one of prior, during and subsequent to the executing step.

9. A method for operating a clocked integrated semiconductor circuit, the method which comprises:

executing, in a first circuit unit of an integrated semiconductor circuit, an operation which requires a given number of clock signal periods of a clock signal; and

activating, during the executing step, at least a second circuit unit for a duration of time periods determined by a random signal by supplying one of the clock signal and a further clock signal to the second circuit unit.

10. The method according to claim 9, which comprises interrupting during at least one of the time periods determined by the random signal, the operation executed in the first circuit unit.

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COMBINED DECLARATION AND POWER OF ATTORNEY IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CLOCKED INTEGRATED SEMICONDUCTOR CIRCUIT AND METHOD FOR OPERATING SUCH A CIRCUIT

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

European Patent Application No. 98114199.7, filed July 29, 1998, the International Priority of which is claimed under 35 U.S.C. §119; and International Application No. PCT/EP99/05391, filed July 27, 1999, the Priority of which is claimed under 35 U.S.C. §120.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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